3MHz 1A Step-Down Converter

General Description

The RT8048 is a high-efficiency Pulse-Width-Modulated (PWM) step-down DC/DC converter. Capable of delivering 1A output current over a wide input voltage range from 2.5V to 5.5V, the RT8048 is ideally suited for portable electronic devices that are powered from 1-cell Li-ion battery or from other power sources such as cellular phones, PDAs and hand-held devices. Two operating modes are available including : PWM/Low Dropout auto switch and shut-down mode. The internal synchronous rectifier with low $R_{DS(ON)}$ dramatically reduces conduction loss at PWM mode. No external Schottky diode is required in practical application. The RT8048 enters Low-Dropout mode when normal PWM cannot provide regulated output voltage by continuously turning on the upper P-MOSFET. The RT8048 enters shut-down mode and consumes less than 0.1μA when EN pin is pulled low. The switching ripple is easily smoothed-out by small package filtering elements due to a fixed operating frequency of 3MHz.

Ordering Information

RT8048(-□□)□□

Package Type
QW : WDFN-6L 2x2 (W-Type)

Lead Plating System
Z : ECO (Ecological Element with Halogen Free and Pb free)

Output Voltage
Default : Adjustable
10 : 1.0V
12 : 1.2V
15 : 1.5V
18 : 1.8V
25 : 2.5V
33 : 3.3V

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

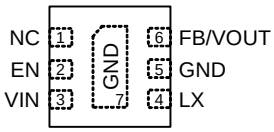
- **2.5V to 5.5V Input Range**
- **3MHz Fix-Frequency PWM Operation**
- **1A Output Current**
- **90% Efficiency**
- **No Schottky Diode Required**
- **0.6V Reference Allows Low Output Voltage**
- **Low Dropout Operation : 100% Duty Cycle**
- **RoHS Compliant and Halogen Free**

Applications

- Portable Instruments
- Microprocessors and DSP Core supplies
- Cellular Phones
- Wireless and DSL Modems
- PC Cards

Pin Configurations

(TOP VIEW)



WDFN-6L 2x2

Marking Information

HB : Product Code
W : Date Code

Typical Application Circuit

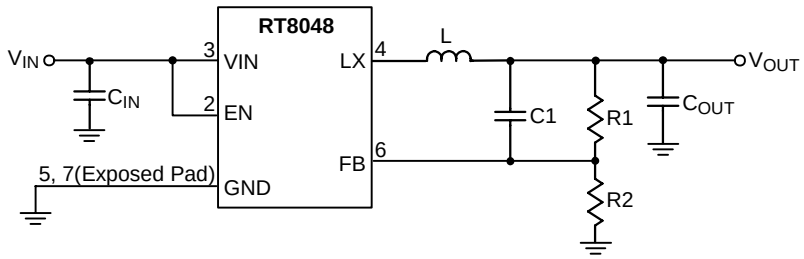


Figure 1. Adjustable Voltage Regulator

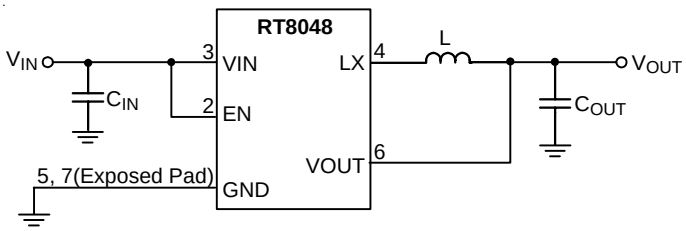


Figure 2. Fixed Voltage Regulator

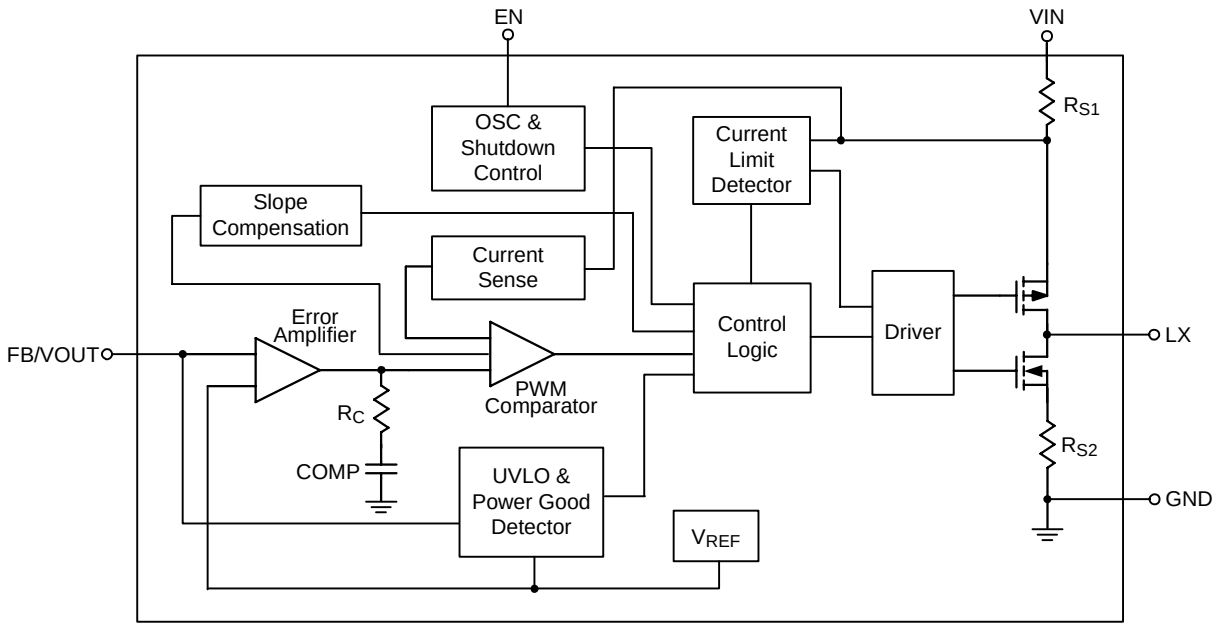
Table 1. Recommended Component Selection

V_{OUT} (V)	L (µH)	R1 (kΩ)	R2 (kΩ)	C_{OUT} (µF)
1.2	0.47	82	82	4.7
1.8	0.47	100	49.9	4.7
2.5	1	91	28.7	4.7
3.3	1	82	18	10

Function Pin Description

Pin No.		Pin Name	Pin Function
Adjustable Output Voltage	Fixed Output Voltage		
1	1	NC	No Internal Connection.
2	2	EN	Chip Enable (Active High).
3	3	VIN	Power Input.
4	4	LX	Switch Node.
5, 7 (Exposed Pad)	5, 7 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
6	--	FB	Feedback.
--	6	VOUT	Output Voltage.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, V_{IN} ---------- 6.5V
- Power Dissipation, P_D @ T_A = 25°C
  WDFN-6L 2x2 ---------- 0.833W
- Package Thermal Resistance (Note 2)
  WDFN-6L 2x2, θ_{JA} ---------- 120°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM ---------- 2kV
  MM ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, V_{IN} ---------- 2.5V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 3.6V, T_A = 25°C unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Current		I_Q		--	81	--	μA
Reference Voltage		V_{REF}		0.588	0.6	0.612	V
Under Voltage Lockout Threshold		V_{UVLO}	V_{IN} Rising	--	2.3	--	V
			V_{IN} Falling	--	2.1	--	
Shutdown Current		I_{SHDN}		--	0.1	1	μA
Switching Frequency		f_{OSC}		--	3	--	MHz
EN Input Threshold Voltage	Logic-High	V_{IH}		1.5	--	V_{IN}	V
	Logic-Low	V_{IL}		--	--	0.4	
Thermal Shutdown Temperature		T_{SD}		--	140	--	°C
Switch On Resistance, High		R_{PFET}	I_{LX} = 0.2A	--	250	--	mΩ
Switch On Resistance, Low		R_{NFET}	I_{LX} = 0.2A	--	260	--	mΩ
Peak Current Limit		I_{LIM}		--	1.5	--	A
Output Voltage Line Regulation			V_{IN} = 2.5V to 5.5V	--	--	1	%/V
Output Voltage Load Regulation			0mA < I_{LOAD} < 0.6A	--	--	1	%

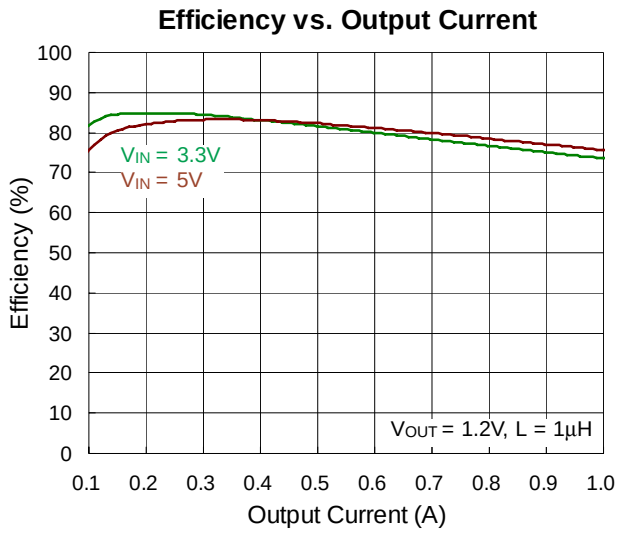
Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

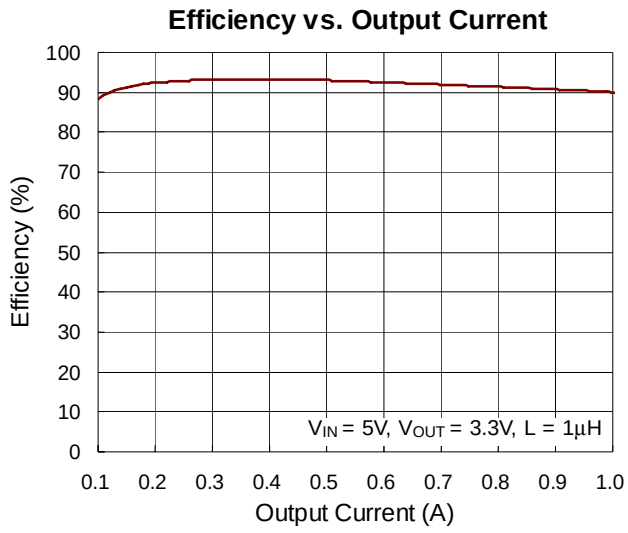
Note 2. θ_{JA} is measured in natural convection at T_A = 25°C on a high effective thermal conductivity four-layer test board of JEDEC 51-7 thermal measurement standard.

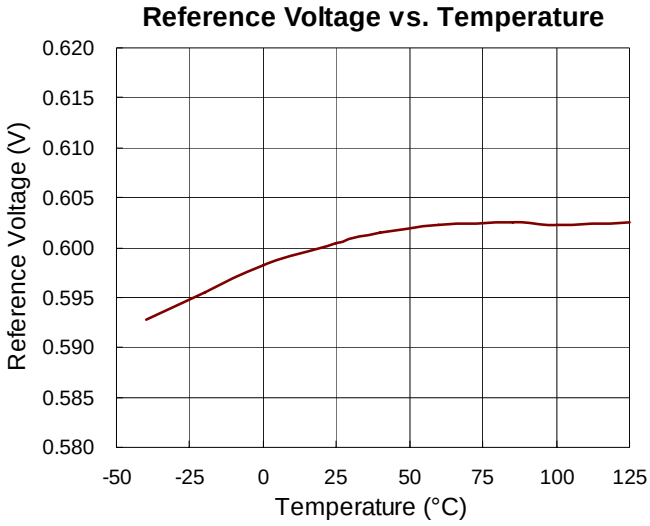
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

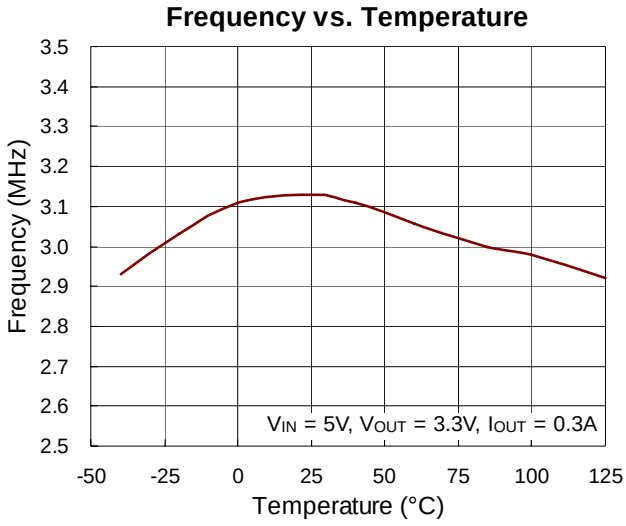
Note 4. The device is not guaranteed to function outside its operating conditions.

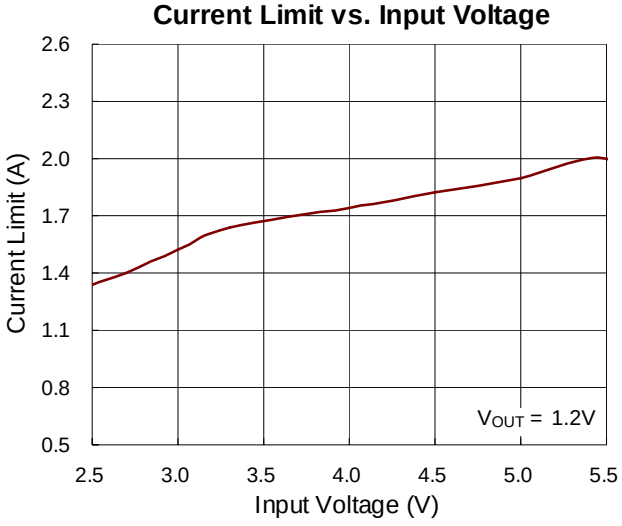
Typical Operating Characteristics

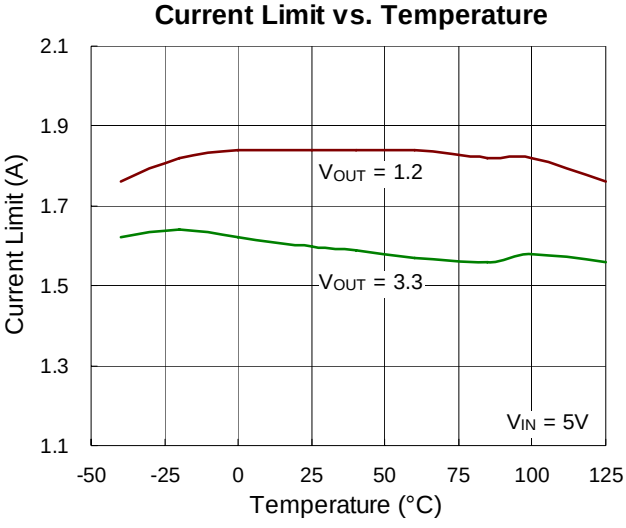




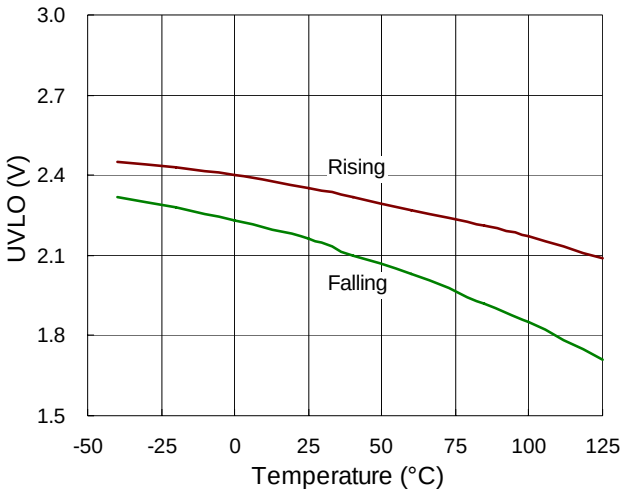




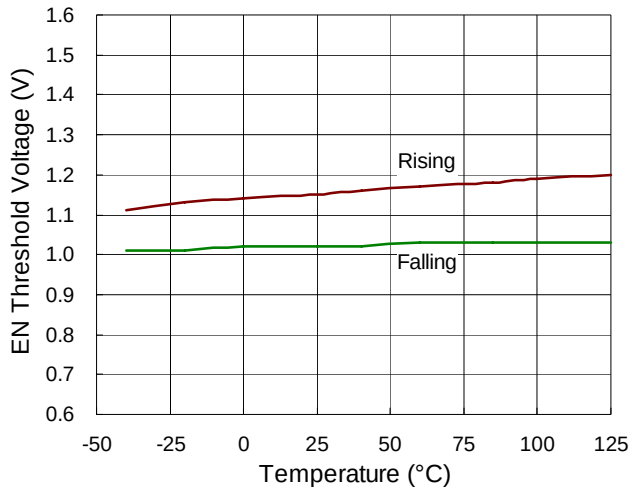




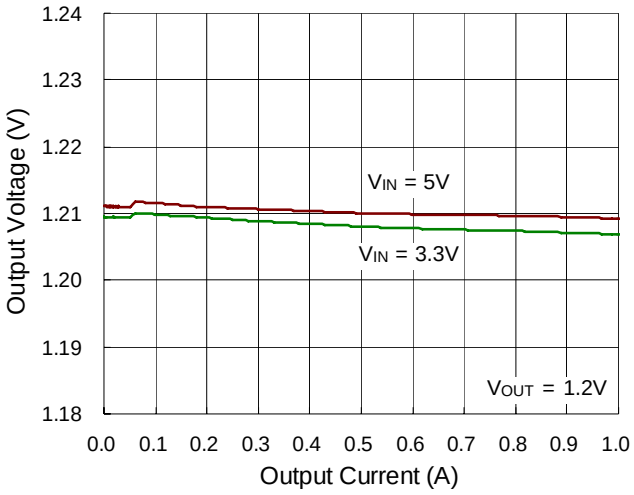
UVLO vs. Temperature



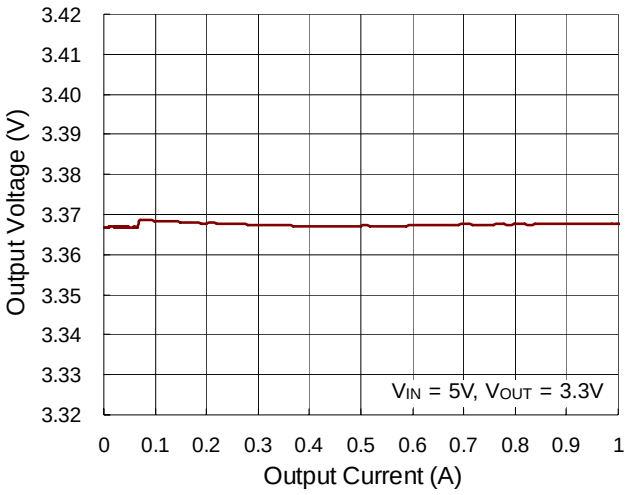
EN Threshold Voltage vs. Temperature



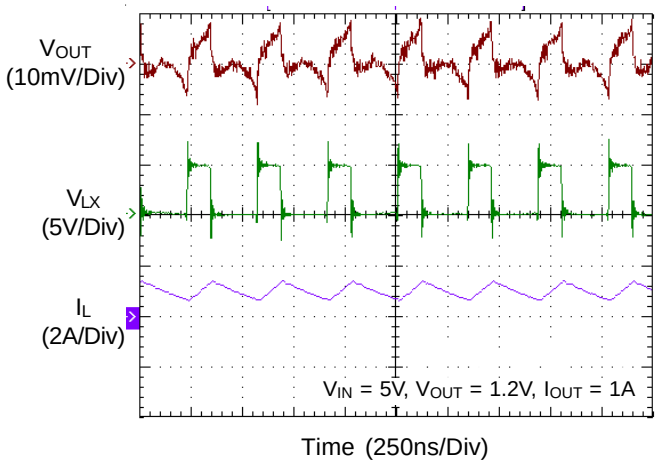
Output Voltage vs. Output Current



Output Voltage vs. Output Current



Switching



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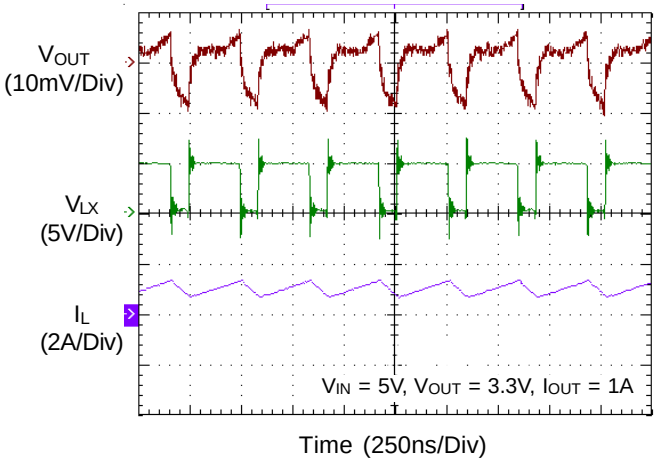
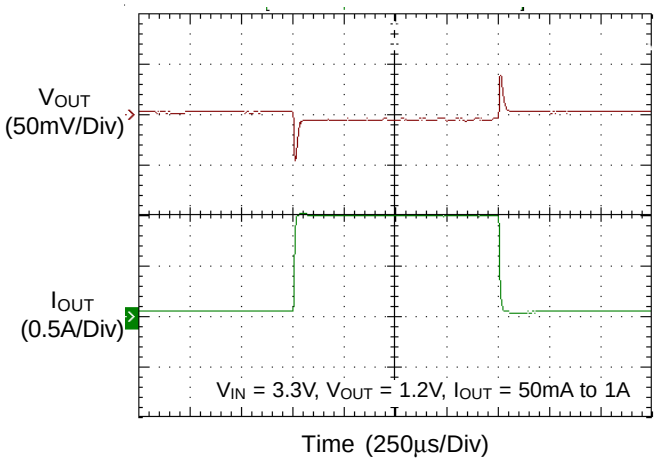
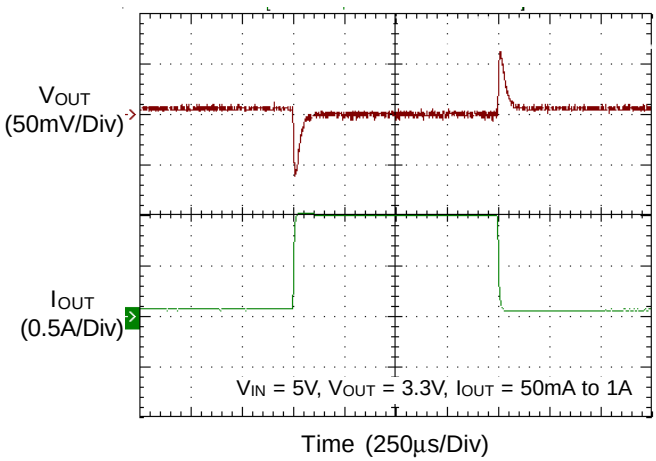


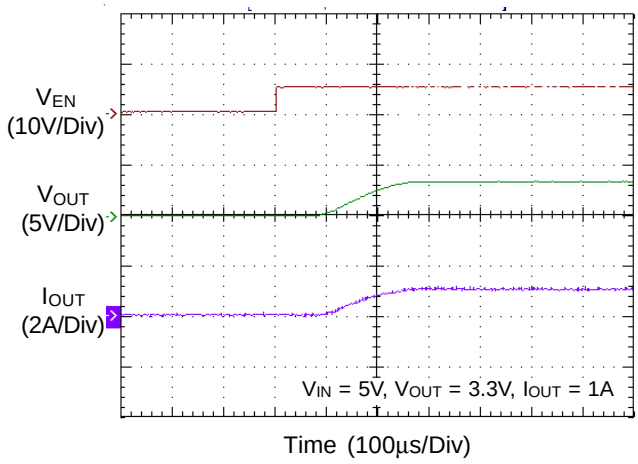
Load Transient Response



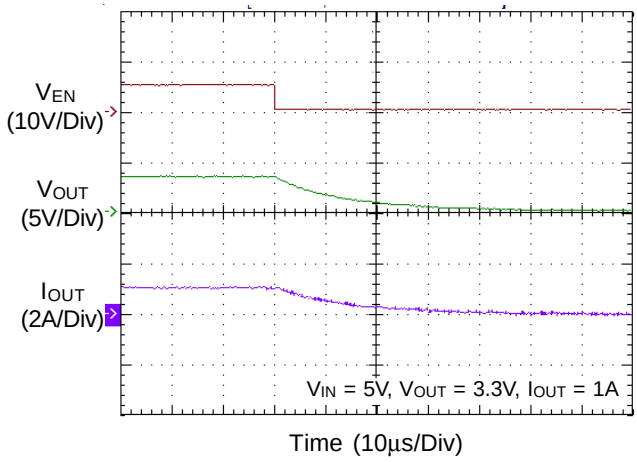
Load Transient Response



Power On from EN



Power Off from EN



Application Information

The basic RT8048 application circuit is shown in Typical Application Circuit. External component selection is determined by the maximum load current and begins with the selection of the inductor value and operating frequency followed by C_{IN} and C_{OUT}. Although frequency as high as 3MHz are possible, the minimum on-time of the RT8048 imposes a minimum limit on the operating duty cycle. The minimum duty is equal to 70ns' f_{OSC}(Hz)' 100%.

Inductor Selection

For a given input and output voltage, the inductor value and operating frequency determine the ripple current. The ripple current ΔI_L increases with higher V_{IN} and decreases with higher inductance :

$$\Delta I_L = \left[\frac{V_{OUT}}{f_{OSC} \times L}\right]\left[1-\frac{V_{OUT}}{V_{IN}}\right]$$

Having a lower ripple current reduces the ESR losses in the output capacitors and the output voltage ripple. Highest efficiency operation is achieved at low frequency with small ripple current. This, however, requires a large inductor. A reasonable starting point for selecting the ripple current is ΔI_L = 0.4 (I_{MAX}). The largest ripple current occurs at the highest V_{IN}. To guarantee that the ripple current stays below a specified maximum, the inductor value should be chosen according to the following equation :

$$L = \left[\frac{V_{OUT}}{f_{OSC} \times \Delta I_{L(MAX)}}\right]\left[1-\frac{V_{OUT}}{V_{IN(MAX)}}\right]$$

Inductor Core Selection

Once the value for L is known, the type of inductor can be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite or molypermalloy cores. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on the inductance selected. As the inductance increases, core losses decrease. Unfortunately, increased inductance requires more turns of wire and, therefore, more copper losses. Ferrite designs have very low core losses and are preferred at high switching frequencies. Hence, design goals should concentrate on copper loss and saturation prevention. Ferrite core material saturates " hard" , which means that the inductance collapses abruptly when the peak design current is exceeded. This result in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate! Different core materials and shapes will change the size, current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate energy, but generally cost more than powdered iron core inductors with similar characteristics. The choice of inductor type to use mainly depends on the price vs. size requirements and any radiated field/EMI requirements.

C_{IN} and C_{OUT} Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal current at the source of the top MOSFET. To prevent large ripple voltage, a low ESR input capacitor sized for the maximum RMS current should be used. RMS current is given by :

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life, which makes it advisable to either further derate the capacitor or choose a capacitor rated at a higher temperature than required. Several capacitors may also be placed in parallel to meet size or height requirements in the design. The selection of C_{OUT} is determined by the effective series resistance (ESR) that is required to minimize voltage ripple and load step transients, as well as the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be examined by viewing the load transient response as described in a later section. The output ripple, ΔV_{OUT}, is determined by :

$$\Delta V_{OUT} \leq \Delta I_L \left[ESR + \frac{1}{8 f_{OSC} C_{OUT}}\right]$$

The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special

polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR, but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density, but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR but can be used in cost sensitive applications provided that consideration is given to ripple current ratings and long term reliability. Ceramic capacitors have excellent low ESR characteristics, but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing.

Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, VIN. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at VIN large enough to damage the part.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to ΔI_{LOAD} (ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT}, generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing, which would indicate a stability problem.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications of the RT8048, the maximum junction temperature is 125°C and T_A is the ambient temperature. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WDFN-6L 2x2 packages, the thermal resistance, θ_{JA}, is 120°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (120°C/W) = 0.833W for WDFN-6L 2x2 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. For the RT8048 packages, the derating curve in Figure 3 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

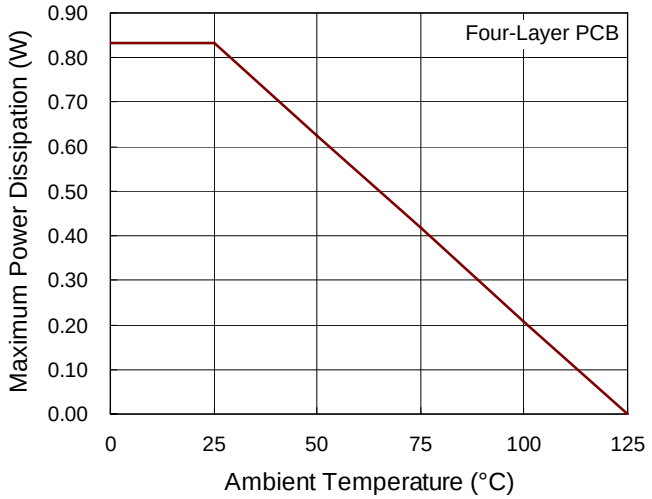
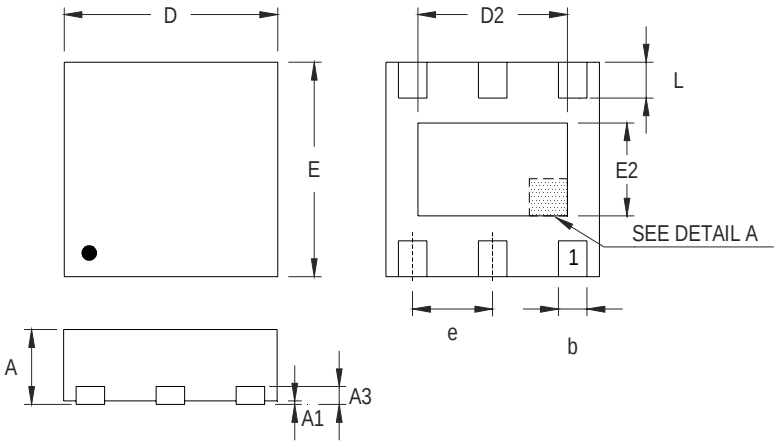
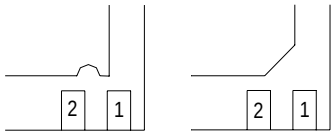


Figure 3. Derating Curve for the RT8048 Packages

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.350	0.008	0.014
D	1.950	2.050	0.077	0.081
D2	1.000	1.450	0.039	0.057
E	1.950	2.050	0.077	0.081
E2	0.500	0.850	0.020	0.033
e	0.650		0.026	
L	0.300	0.400	0.012	0.016

W-Type 6L DFN 2x2 Package

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